NOVOSENSE
纳芯微电子

NSi1050
Isolated CAN Transceiver
Datasheet (EN) 1.5

Product Overview

The NSi1050 is a isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSi1050 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSi1050 device is safety certified by UL1577 support 5kV$_{rms}$ insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NSi1050 is up to 1Mbps. The NSi1050 provides thermal protection and transmit data dominant time out function.

Key Features

- Fully compatible with the ISO11898-2 standard
- Up to 5000Vrms Insulation voltage
- Power supply voltage

  VDD1: 2.5V to 5.5V

  VDD2: 4.5V to 5.5V
- Bus fault protection of -40V to +40V
- Transmit data (TXD) dominant time out function
- Over current and over temperature protection
- Date rate: up to 1Mbps
- High CMTI: 100kV/us
- Low loop delay: <200ns
- High system level EMC performance:
  Enhanced system level ESD, EFT, Surge immunity
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  -SOW16
  -DUB8

Safety Regulatory Approvals

- UL recognition: up to 5000Vrms for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

Applications

- Industrial automation system
- Isolated CAN Bus
- Telecom

Device Information

Part Number	Package	Body Size
NSi1050-DDBR	DUB8	9.30mm ×6.40mm
NSi1050-DSWR	SOW16	10.30mm × 7.50mm

Functional Block Diagrams

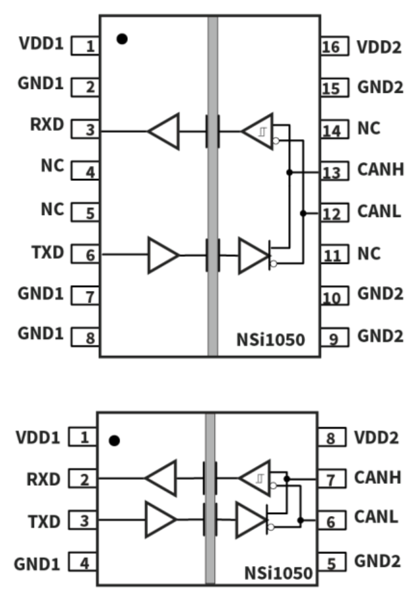

Figure 1. NSi1050 Block Diagram

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1. Pin Configuration and Functions

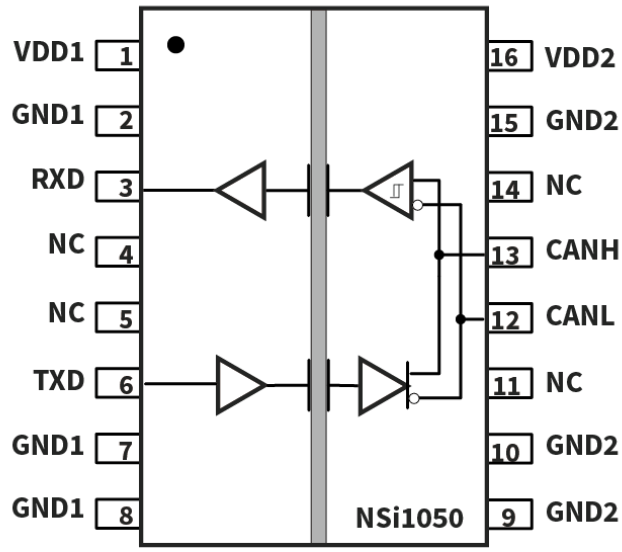


Figure 1.1 NSi1050-DSWR Package

Table1.1 NSi1050-DSWR Pin Configuration and Description

NSi1050-DSWR PIN NO.	SYMBOL	FUNCTION
1	VDD_1	Power Supply for Side 1
2	GND_1	Ground 1, the ground reference for Isolator Side 1
3	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
4	NC	No Connection
5	NC	No Connection
6	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
7	GND_1	Ground 1, the ground reference for Isolator Side 1
8	GND_1	Ground 1, the ground reference for Isolator Side 1
9	GND_2	Ground 2, the ground reference for Isolator Bus Side
10	GND_2	Ground 2, the ground reference for Isolator Bus Side
11	NC	No Connection
12	CANL	Low-level CAN bus line
13	CANH	High-level CAN bus line
14	NC	No Connection
15	GND_2	Ground 2, the ground reference for Isolator Bus Side
16	VDD_2	Power supply for Bus Side

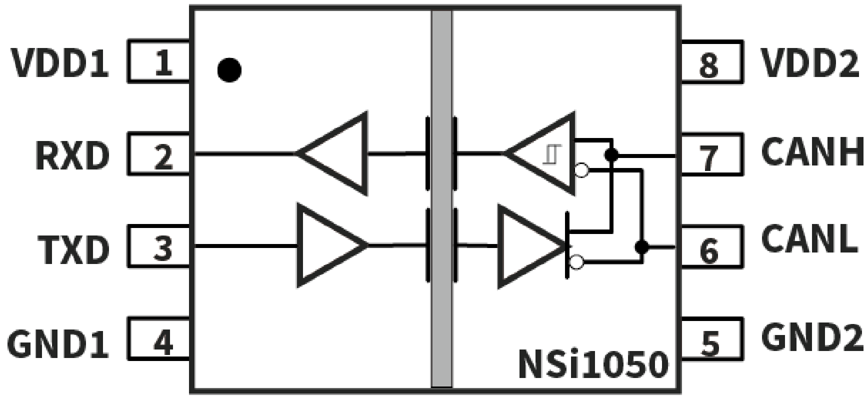


Figure 1.2 NSi1050-DDBR Package

Table1.2 NSi1050-DDBR Pin Configuration and Description

NSi1050-DDBR PIN NO.	SYMBOL	FUNCTION
1	VDD_1	Power Supply for Side 1
2	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
3	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
4	GND_1	Ground 1, the ground reference for Isolator Side 1
5	GND_2	Ground 2, the ground reference for Isolator Bus Side
6	CANL	Low-level CAN bus line
7	CANH	High-level CAN bus line
8	VDD_2	Power supply for Bus Side

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD_1, VDD_2	-0.5		6.5	V	
Maximum Input Voltage	V_{TXD}	-0.4		VDD_1+0.4	V	
Maximum BUS Pin Voltage	V_{CANH}, V_{CANL}	-40		+40	V	
Output current	Io	-15		15	mA	
Operating Temperature	Topr	-40		125	℃	
Storage Temperature	Tstg	-40		150	℃	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply voltage, controller side	V_{CC1}	2.5		5.5	V	
Supply voltage, bus side	V_{CC2}	4.5	5	5.5	V	
Voltage at bus pins (separately or common mode)	V_I or V_{IC}	-12		12	V	
High-level input voltage	V_{IH}	2		5.25	V	TXD
Low-level input voltage	V_{IL}	0		0.8	V	TXD
High-level output current	I_{OH}	-70			mA	Driver
		-4			mA	Receiver
Low-level output current	I_{OL}			70	mA	Driver
				4	mA	Receiver
Ambient Temperature	T_A	-40		125	℃	
Junction temperature	T_J	-40		150	℃	

4. Thermal Information

Parameters	Symbol	DUB8	SOW16	Unit
Junction-to-ambient thermal resistance	θ_{JA}	73.3	76.0	℃/W
Junction-to-case(top) thermal resistance	$\theta_{JC(top)}$	63.2	41	
Junction-to-board thermal resistance	θ_{JB}	43.0	47.7	

5. Specifications

5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=4.5V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage	VDD_1	2.5		5.5	V	
	VDD_2	4.5	5	5.5	V	
Logic side supply current	IDD_1		1.97	3.00	mA	VDD_1=3.3V, TXD=0
			0.97	1.50	mA	VDD_1=3.3V, TXD=VCC1
			2.02	3.00	mA	VDD_1=5V, TXD=0
			1.02	1.50	mA	VDD_1=5V, TXD=VCC1
Bus side supply current	IDD_2		46	70	mA	TXD=0V, R_{Load} =60Ω
			4.45	10	mA	TXD=VDD_2
Thermal-Shutdown Threshold	T_{TS}	155	165	180	℃	
Common Mode TraNSient Immunity	CMTI	±80	±100		kV/us	
Logic Side						
High level input voltage	V_{IH}	2			V	TXD pin
Low level input voltage	V_{IL}			0.8	V	TXD pin
High level input current	I_{IH}			10	uA	TXD pin
Low level input current	I_{IL}	-10			uA	TXD pin
Output Voltage High	V_{OH}	VDD_1-0.4			V	I_{OH} = -4mA, RXD pin
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 4mA, RXD pin
Input Capacitance	C_{IN}		2		pF	TXD pin
Driver						
CANH output voltage (Dominant)	$V_{OH(D)}$	2.8	3.44	4	V	VI=0V, R_{Load} =60Ω
CANL output voltage (Dominant)	$V_{OL(D)}$	0.8	1.33	2	V	VI=0V, R_{Load} =60Ω
CAN bus output voltage (Recessive)	$V_{O(R)}$	2	2.5	3	V	TXD=VCC1, R_{Load} =60Ω
Differential output voltage (Dominant)	$V_{OD(D)}$	1.5		3	V	TXD=0, R_{Load} =60Ω
		1		3		TXD=0, RLoad =45Ω
Differential output voltage (Recessive)	$V_{OD(R)}$	-0.12		0.012	V	TXD=VCC1, R_{Load} =60Ω, see Figure 2.1
		-0.5		0.05	V	TXD=VCC1, NO Load
Common-mode output voltage	V_{OC}	2	2.5	3	V	
Peak-to-peak Common-mode output voltage	$V_{OC(PP)}$		250		mV	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Short- circuit output current	I_{OS}	-105	-44.1		mA	CANH=-12V, CANL open, see Figure 5.10
			0.28	1	mA	CANH=12V, CANL open, see Figure 5.10
		-1	-0.44		mA	CANL=-12V, CANH open, see Figure 5.10
			42.5	105	mA	CANL=12V, CANH open, see Figure 5.10
Receiver						
Positive-going bus input threshold voltage	V_{IT+}		750	900	mV	
Negative-going bus input threshold voltage	V_{IT-}	500	650		mV	
Hysteresis voltage	V_{HYS}		100		mV	
Input capacitance to ground	C_I		13		pF	CANH or CANL
Differential input	C_{ID}		5		pF	
Differential input resistance	R_{ID}	30		80	kΩ	
Input resistance	R_{IN}	15	30	40	kΩ	
Input resistance matching	RI_{match}	-3		+3	%	CANH=CANL
Common-mode voltage range	V_{COM}	-12		+12	V	

5.2. Switching Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=4.5V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Loop delay1	T_{loop1}	100	165	210	ns	Driver input to receiver output, Recessive to Dominant
Loop delay2	T_{loop2}	80	125	170	ns	Driver input to receiver output, Dominant to Recessive
Driver						
Propagation delay time, dominant -to- recessive output	t_{PLH}		53	140	ns	
Propagation delay time, recessive -to- dominant output	t_{PHL}		78	110	ns	
Differential output signal rise time	t_r		42		ns	
Differential output signal fall time	t_f		32		ns	
Bus dominant time-out time	t_{TXD_DTO}	300	468	700	us	See Figure 5.9
Receiver						
Propagation delay time, low-to-high-level output	t_{PLH}	65	80	150	ns	
Propagation delay time, high-to-low-level output	t_{PHL}	80	100	150	ns	
RXD signal rise time	t_r		3		ns	
RXD signal fall time	t_f		3		ns	
Fail-Safe output delay time from bus-side power loss	t_{fs}		4.2		us	VDD_1=5V

5.3. Parameter Measurement Information

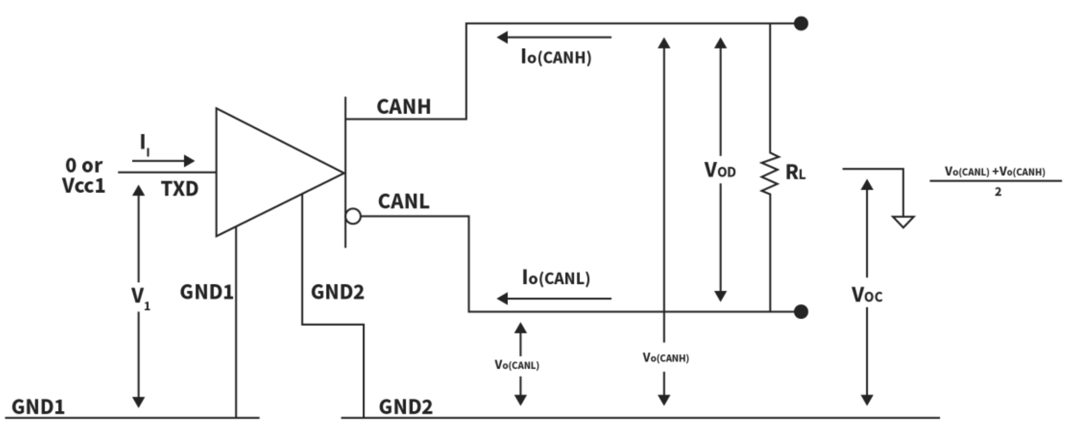


Figure 5.1. Driver Voltage, Current and Test Definitions

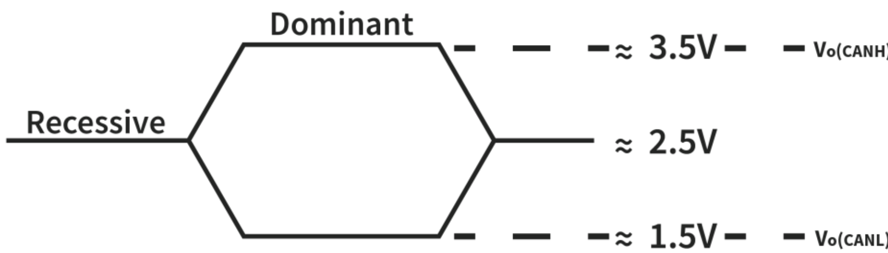


Figure 5.2. Bus Logic State Voltage Definitions

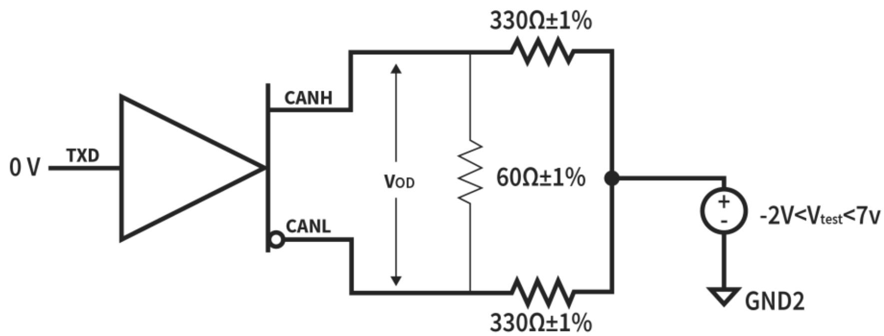
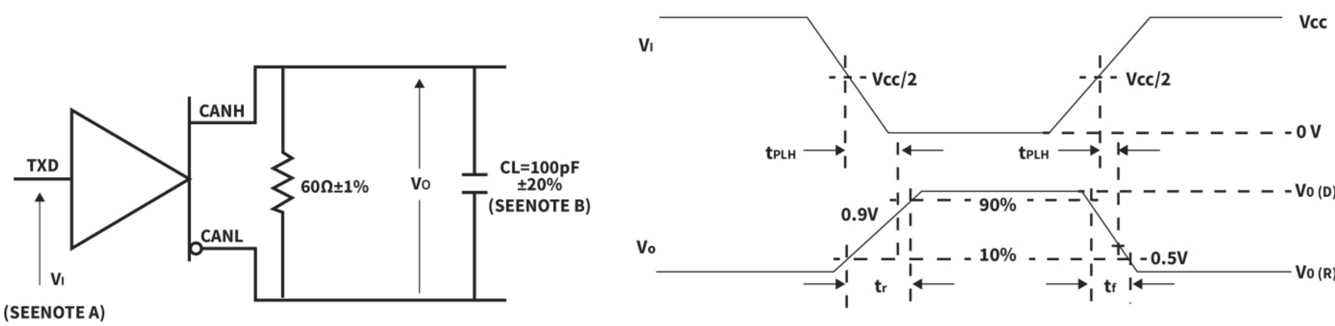


Figure 5.3. Driver VOD With Common-Mode Loading Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, ZO = 50 Ω.
B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 5.4. Driver Test Circuit and Voltage Waveform

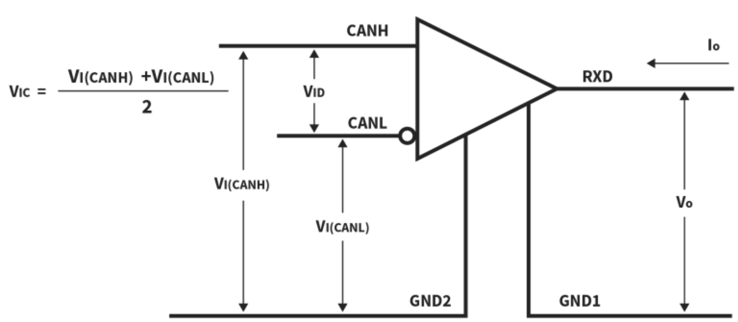
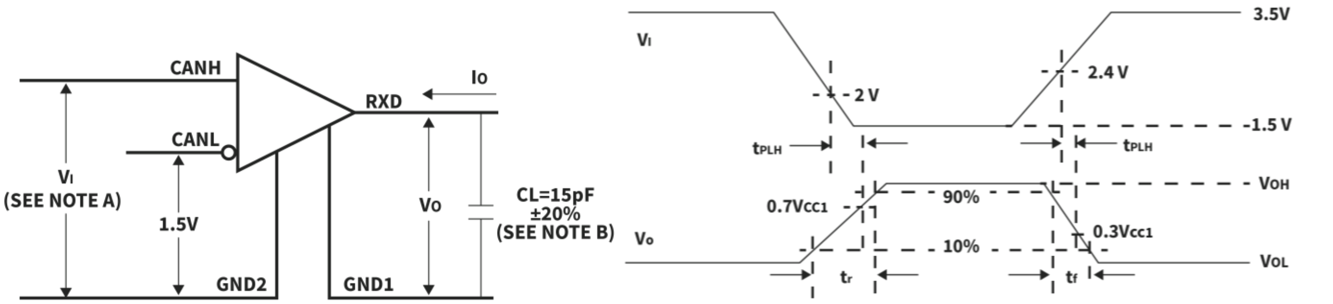


Figure 5.5. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 5.6. Receiver Test Circuit and Voltage Waveform

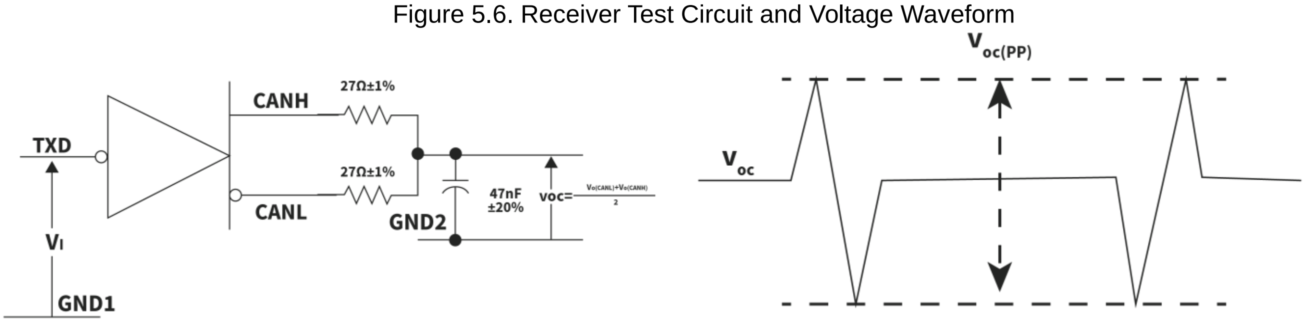


Figure 5.7. Peak-to-Peak Output Voltage Test Circuit and Waveform

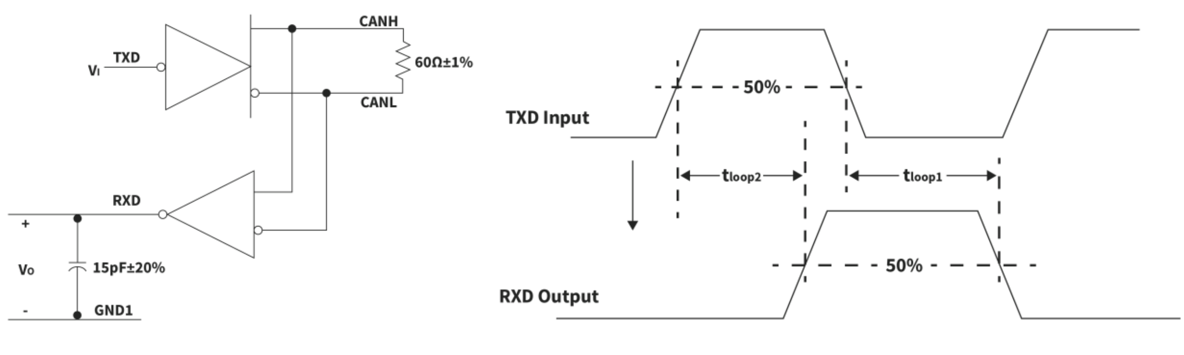
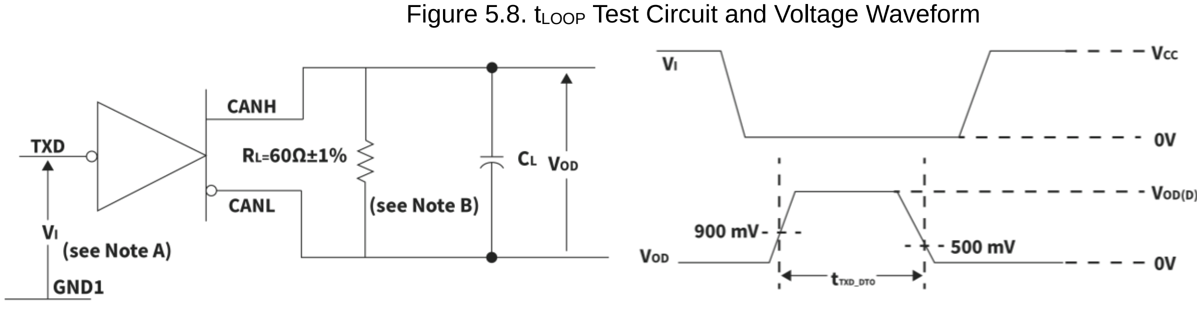


Figure 5.8. t_{LOOP} Test Circuit and Voltage Waveform



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 5.9. Dominant Time-out Test Circuit and Voltage Waveform

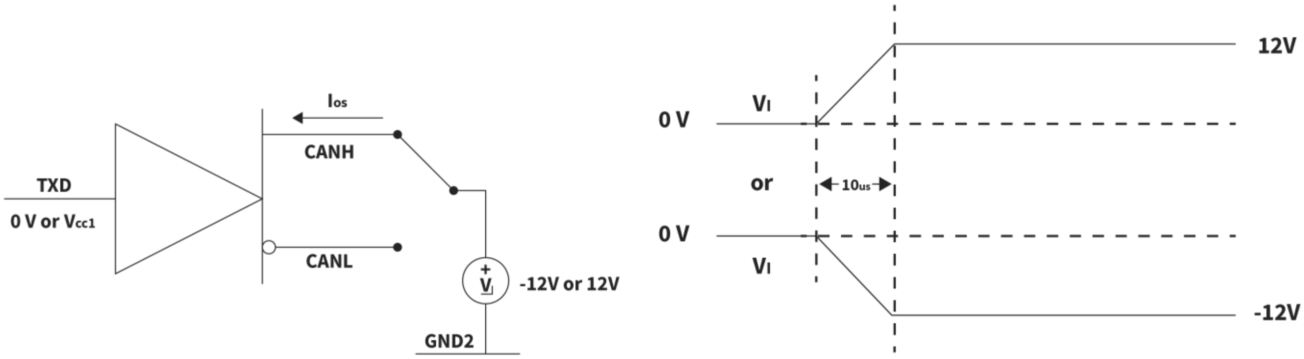


Figure 5.10. Driver Short-Circuit Current Test Circuit and Waveform

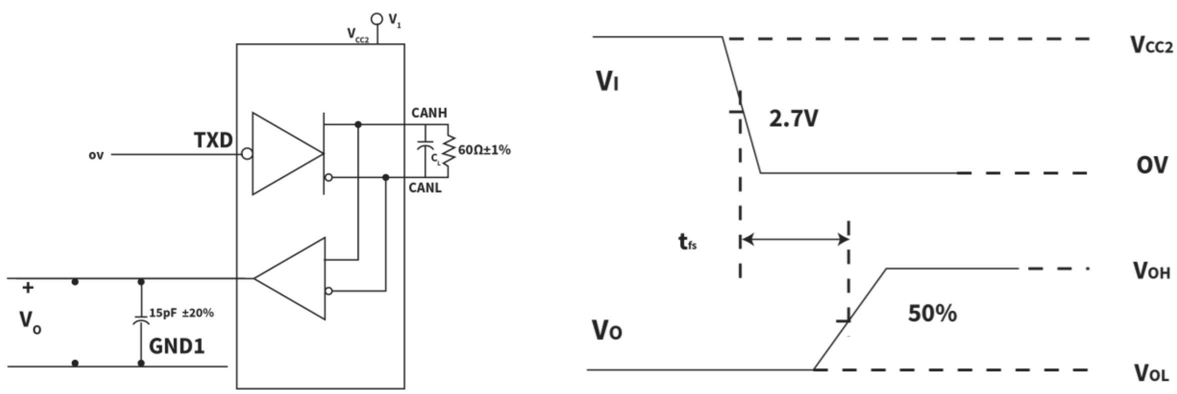


Figure 5.11. Fail-Safe Delay Time Test Circuit and Voltage Waveform

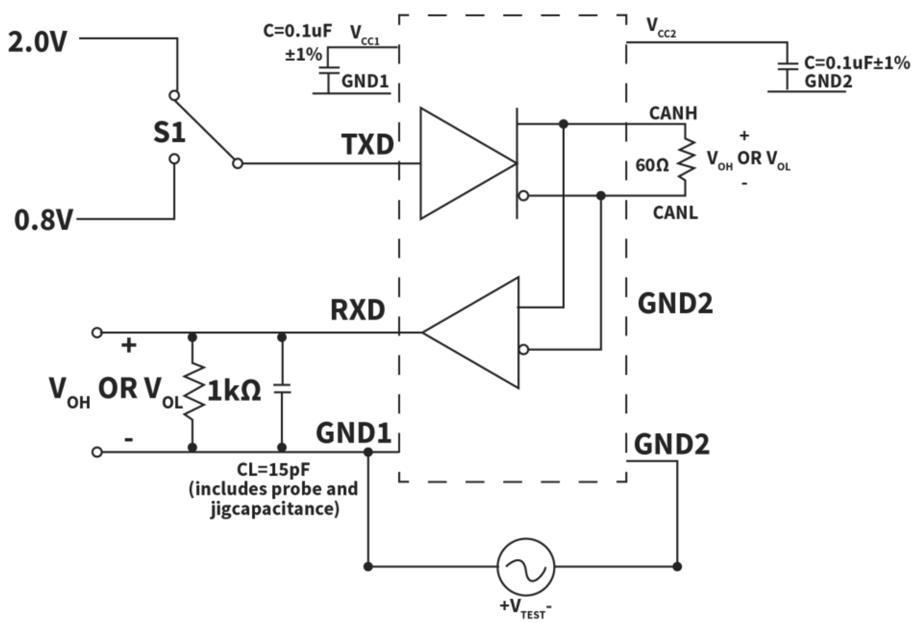


Figure 5.12. Common-Mode TraNSient Immunity Test Circuit

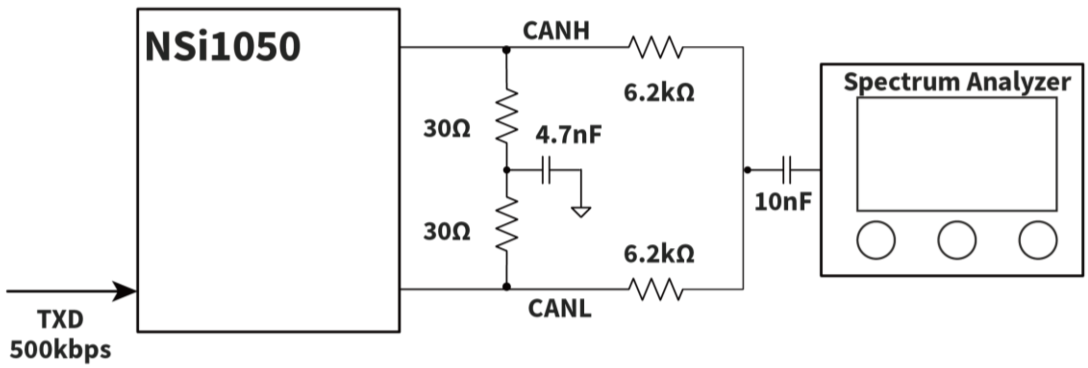


Figure 5.13. Electromagnetic Emissions Measurement Setup

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Description	***Test Condition***	***Symbol***	***Value***		***Unit***
			DUB8	SOW16	
Min. External Air Gap (Clearance)		CLR	6.5	8	mm
Min. External Tracking (Creepage)		CPG	6.5	8	mm
Distance through the Insulation		DTI	20		um
Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	CTI	>400	>600	V
Material Group	IEC 60112		II	I	
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage ≤ 150Vrms			I to IV	I to IV	
For Rated Mains Voltage ≤ 300Vrms			I to III	I to IV	
For Rated Mains Voltage ≤ 600Vrms			I to II	I to IV	
For Rated Mains Voltage ≤ 1000Vrms			I	I to III	
Insulation Specification per DIN VDE V 0884-11:2017-01[1)]					
Climatic Category			10/105/21		
Pollution Degree	per DIN VDE 0110, Table 1		2		
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	400	1500	V_{RMS}
	DC voltage		565	2121	V_{DC}
Maximum Repetitive Isolation Voltage		V_{IORM}	565	2121	V_{peak}
Input to Output Test Voltage, Method B1	$V_{ini.\,b} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.5$, $t_{ini} = t_m = 1$ sec, $q_{pd} \leq 5$ pC,	$V_{pd\,(m)}$	847	\	V_{peak}

Description	Test Condition	Symbol	Value		Unit
	100% production test				
	$V_{ini.\,b} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.875$, $t_{ini} = t_m = 1$ sec, $q_{pd} \leq 5$ pC, 100% production test		\	3977	
Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1	$V_{ini.\,a} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.3$, $t_{ini} = 60$ sec, $t_m = 10$ sec, $q_{pd} \leq 5$ pC	$V_{pd\,(m)}$	678	\	V_{peak}
	$V_{ini.\,a} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.6$, $t_{ini} = 60$ sec, $t_m = 10$ sec, $q_{pd} \leq 5$ pC		\	3394	
Input to Output Test Voltage, Method A. After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{ini.\,a} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.2$, $t_{ini} = 60$ sec, $t_m = 10$ sec, $q_{pd} \leq 5$ pC	$V_{pd\,(m)}$	678	2545	V_{peak}
Maximum Transient Isolation Voltage	t = 60 sec	V_{IOTM}	5300	8000	V_{peak}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = 1.3 \times V_{IOSM}$	V_{IOSM}	5384	\	V_{peak}
	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = 1.6 \times V_{IOSM}$		\	6250	
Isolation Resistance	$V_{IO} = 500$ V, $T_{amb} = T_S$	R_{IO}	$>10^9$		Ω
	$V_{IO} = 500$ V, 100 °C ≤ T_{amb} ≤ 125 °C		$>10^{11}$		Ω
Isolation Capacitance	f = 1MHz	C_{IO}	1.2		pF
Insulation Specification per UL1577					
Withstand Isolation Voltage	$V_{TEST} = 1.2 \times V_{ISO}$, t = 1 sec, 100% production test	V_{ISO}	3000	5000	V_{rms}

1) This coupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

6.2. Safety-Limiting Values

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSi1050-DDBR

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 73.3$ °C/W, $T_J = 150$ °C, $T_A = 25$ °C	1705	mW
Safety Supply Current	$R_{\theta JA} = 73.3$ °C/ W, $V_I = 5$V, $T_J = 150$ °C, $T_A = 25$ °C	341	mA

Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of DUB8 package (Thermal Information Table) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

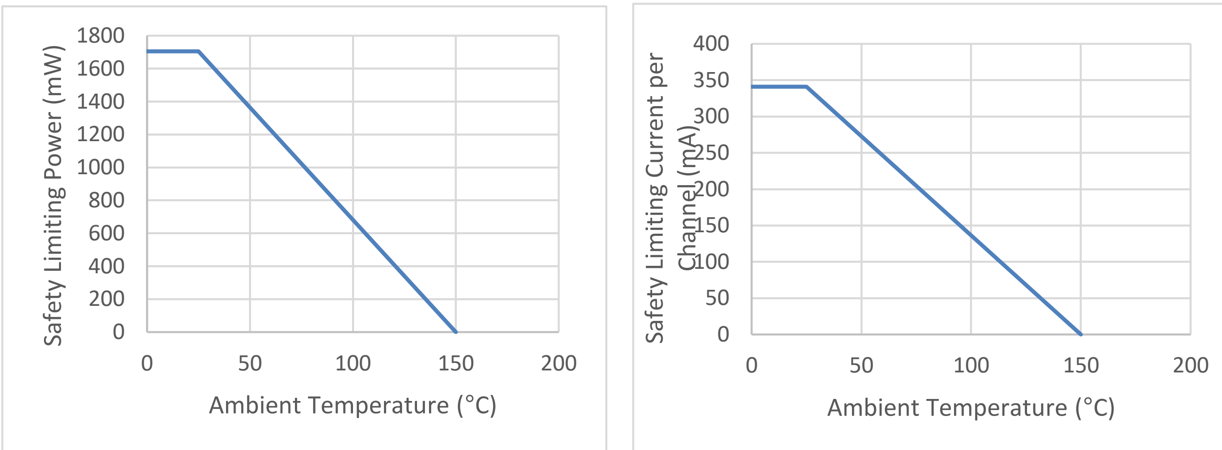


Figure 6.1 NSI1042-DSWVR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSi1050-DSWR

Description	***Test Condition***	***Value***	***Unit***
Safety Supply Power	$R_{\theta JA}$ = 76 °C/W, T_J = 150 °C, T_A = 25 °C	1645	mW
Safety Supply Current	$R_{\theta JA}$ = 76 °C/ W, V_I = 5V, T_J = 150 °C, T_A = 25 °C	329	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP16(300mil) package (Thermal Information Table) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

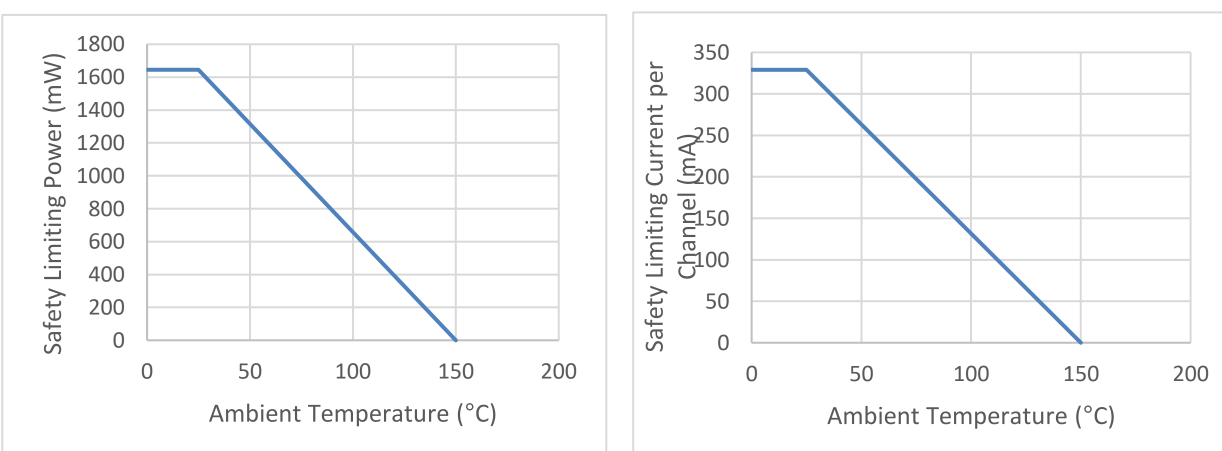


Figure 6.2 NSi1042-DSWR/NSi1052-DSWR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.3. Regulatory information

The NSi1050-DDBR is approved by the organizations listed in table.

CUL		VDE	CQC
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3000V_{rms} Isolation voltage	Single Protection, 3000V_{rms} Isolation voltage	Basic Insulation 565Vpeak, V_{IOSM}=5384Vpeak	Basic insulation
File (E500602)	File (E500602)	File (40050121)	File (CQC20001263786)

The NSi1050-DSWR is approved by the organizations listed in table.

CUL		VDE	CQC
UL 1577 Component Recognition Program1	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-012	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000Vrms Isolation voltage	Single Protection, 5000Vrms Isolation voltage	Reinforced Insulation 2121Vpeak, VIOSM=6250peak	Basic insulation
File (E500602)	File (E500602)	File (pending)	File (CQC20001264939)

7. Function Description

The NSi1050 is a isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSi1050 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSi1050-DSWR device is safety certified by UL1577 support 5kV_{rms} insulation withstand voltages, while the NSi1050-DDBR device is safety certified by UL1577 support 3kV_{rms} insulation withstand voltages. The NSi1050 is providing high electromagnetic immunity and low emissions. The data rate of the NSi1050 is up to 1Mbps. The NSi1050 provides thermal protection and transmit data dominant time out function.

7.1. Device Functional Modes

Table 7.1. Driver Function Table

TXD	CANH	CANL	BUS STATE
L	H	L	Dominant
H	Z	Z	Recessive
Open	Z	Z	Recessive

[1] H= high level; L=low level; Z= common mode(recessive) bias to $V_{CC}/2$

Table 7.2. Receiver Function Table

V_{ID}=CANH-CANL	RXD	BUS STATE
$V_{ID} \geqslant 0.9V$	L	Dominant
0.5< V_{ID} <0.9V	X	Uncertain
$V_{ID} \leqslant 0.5V$	H	Recessive
Open	H	Recessive

[1] H= high level; L=low level; X= uncertain

7.2. TXD dominant time-out function

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.
If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{TXD_DTO}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

7.3. Current Protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

7.4. Over Temperature Protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{TS}, the output drivers will be disabled until the virtual junction temperature becomes lower than T_{TS} and TXD becomes recessive again.
By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

8. Application Note

8.1. Typical Application

The NSi1050 requires a 0.1 µF bypass capacitors between VDD1 and GND1, VDD2and GND2. The capacitor should be placed as close as possible to the package. The figure5.1 is the basic schematic of NSi1050.

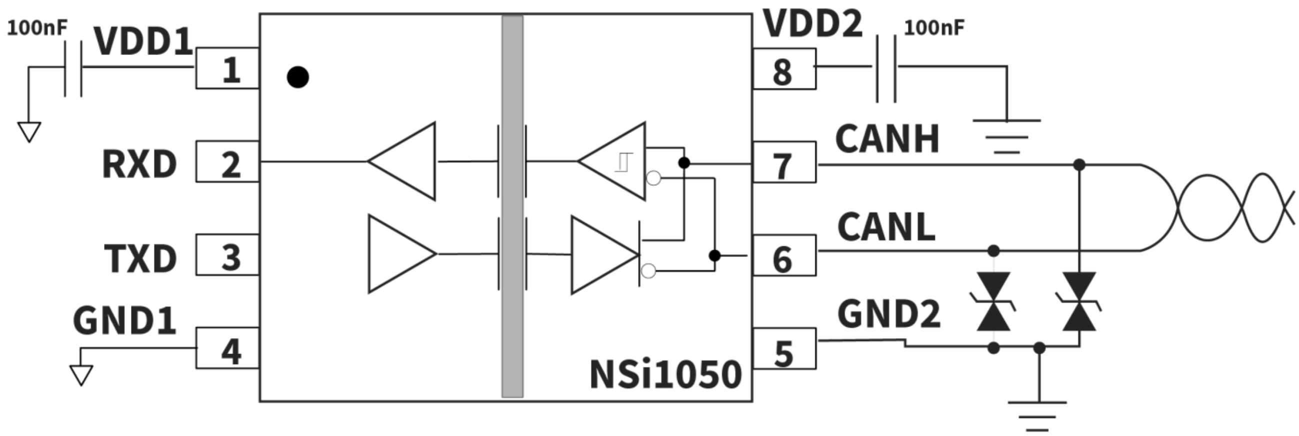


Figure8.1 Basic schematic of NSi1050

8.2. PCB Layout

The recommended PCB layout shown below.

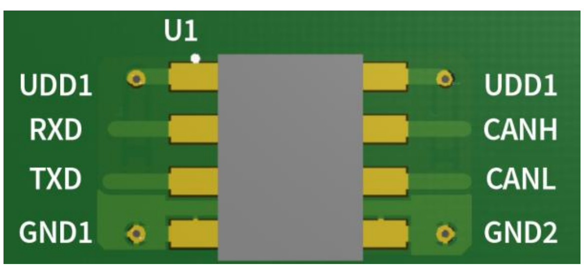
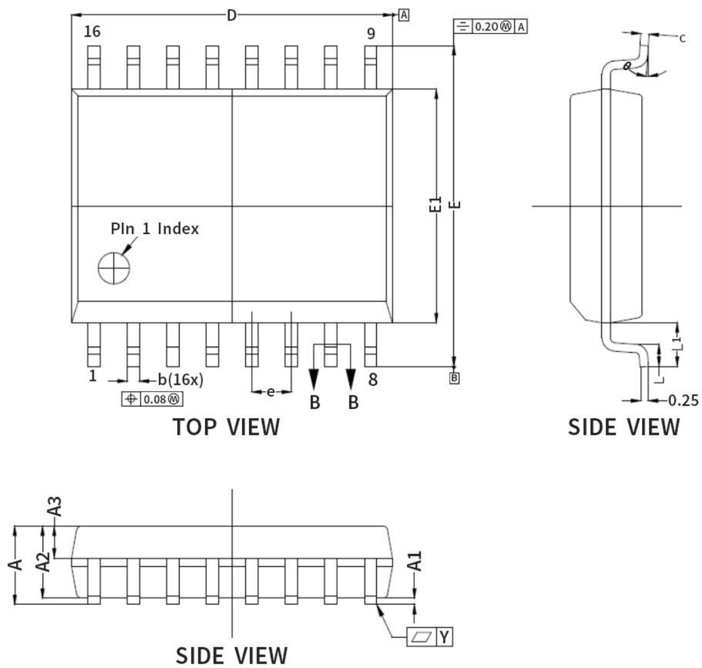


Figure8.2 Recommended PCB Layout — Top Layer

Figure8.3 Recommended PCB Layout — Bottom Layer

9. Package Information



CONTROLLING DIMENSION:MM

Symbol	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

Figure 9.1 SOW16 Package Shape and DimeNSion in millimeters

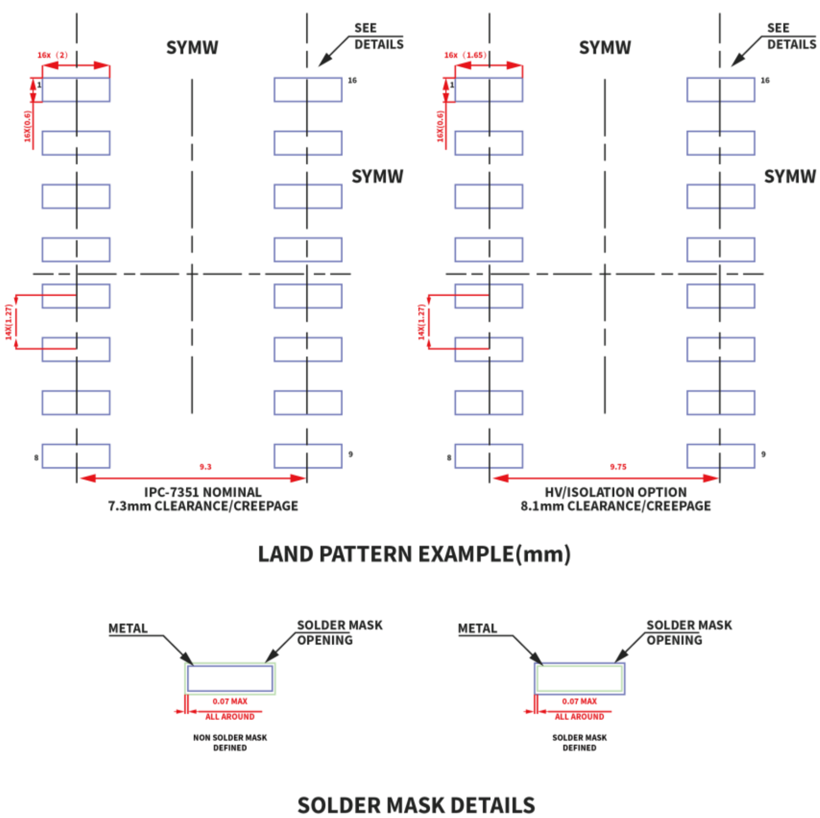
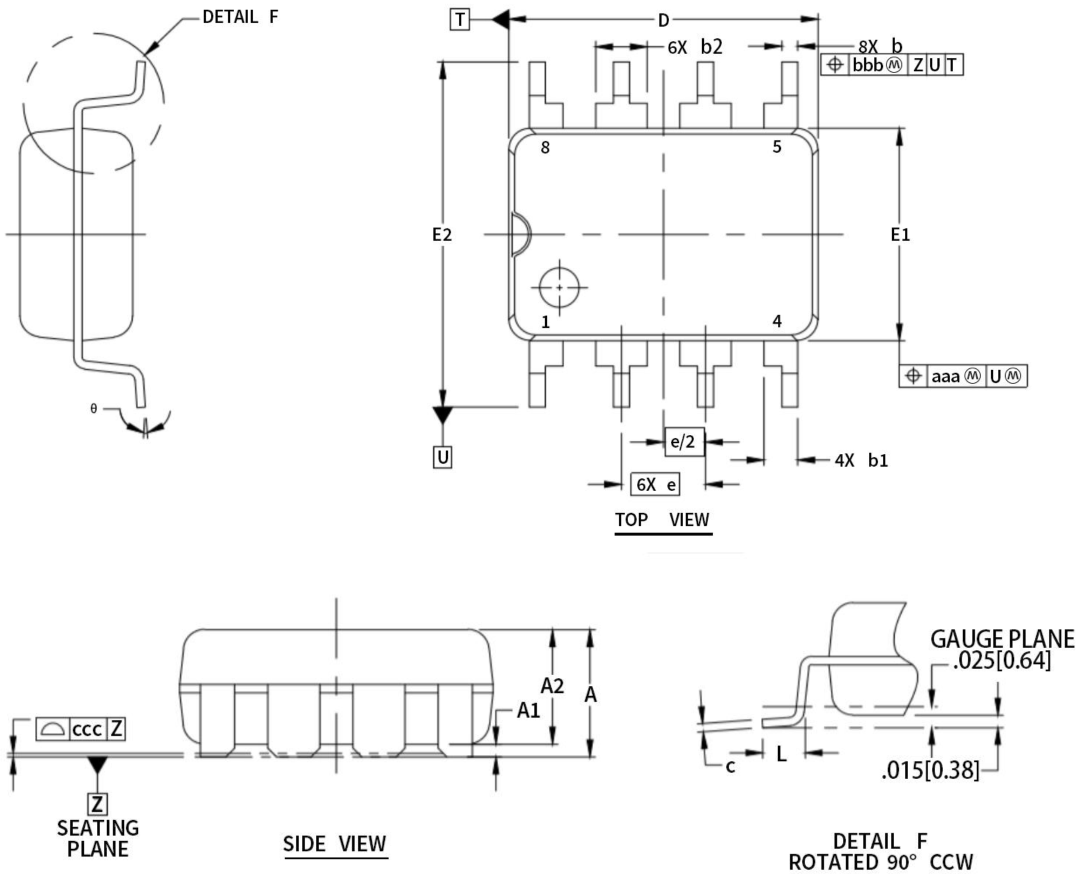


Figure 9.2 SOW16 Package Board Layout Example



	SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS	A	.141	---	.165	3.58	---	4.19
STAND OFF	A1	.015	---	.023	0.38	---	0.58
MOLD THICKNESS	A2	.126	---	.142	3.20	---	3.61
LEAD WIDTH	b	.014	---	.022	0.36	---	0.56
	b1	---	0.039 REF	---	---	0.99 REF	---
	b2	---	0.06 REF	---	---	1.524 REF	---
L/F THICKNESS	c	.008	---	.014	0.20	---	0.36
BODY SIZE	D	.365	---	.369	9.27	---	9.37
	E1	.244	---	.260	6.20	---	6.60
	E2	.398	---	.421	10.11	---	10.69
LEAD PITCH	e	100 BSC			2.54 BSC		
LEAD LENGTH	L	.0453	---	.0571	1.15	---	1.45
	θ	0°	---	8°	0°	---	8°
LEAD OFFSET	aaa	.010			0.254		

Figure 9.3 DUB8 Package Shape and DimeNSion in millimeters

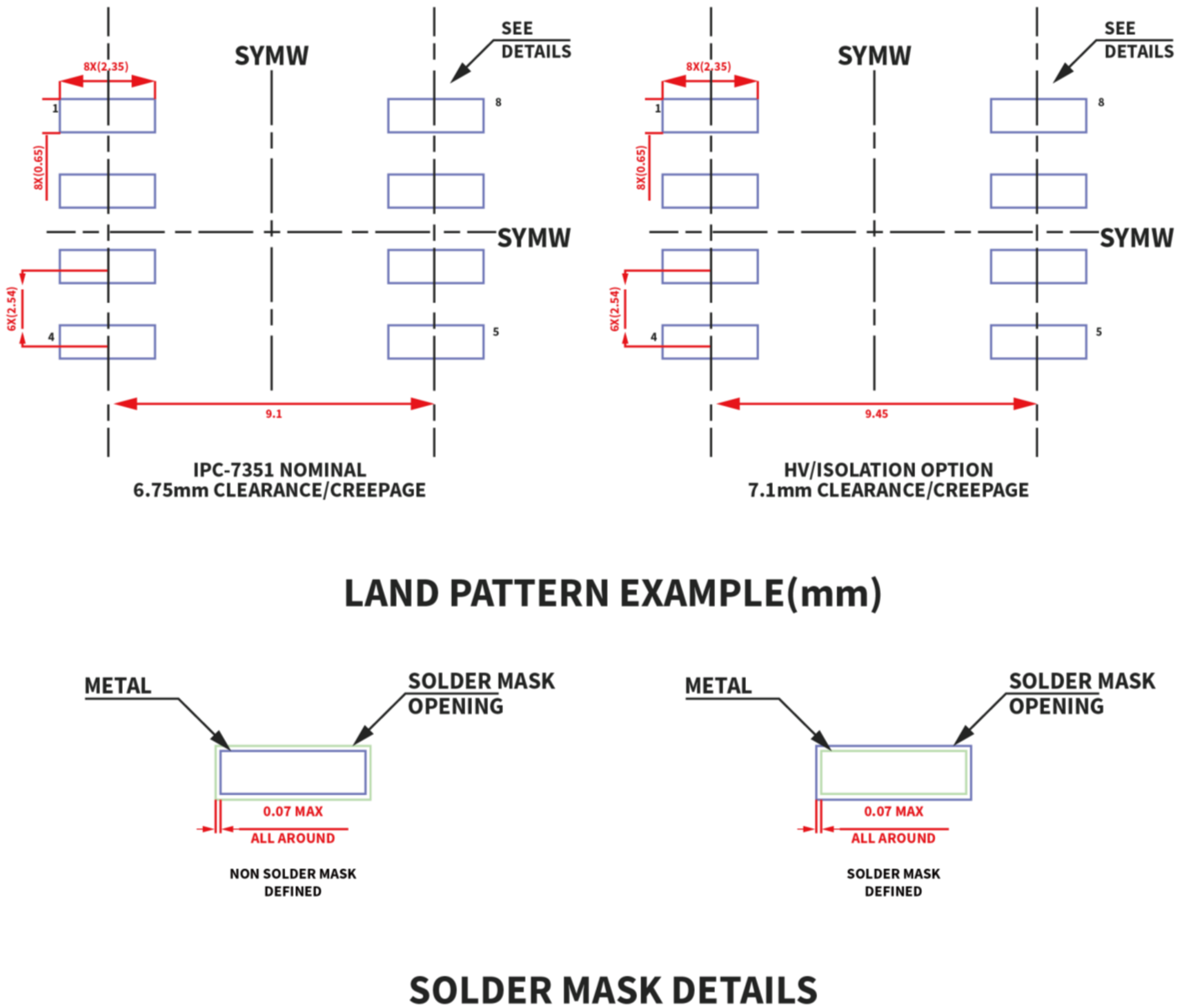


Figure 9.4 DUB8 Package Board Layout Example

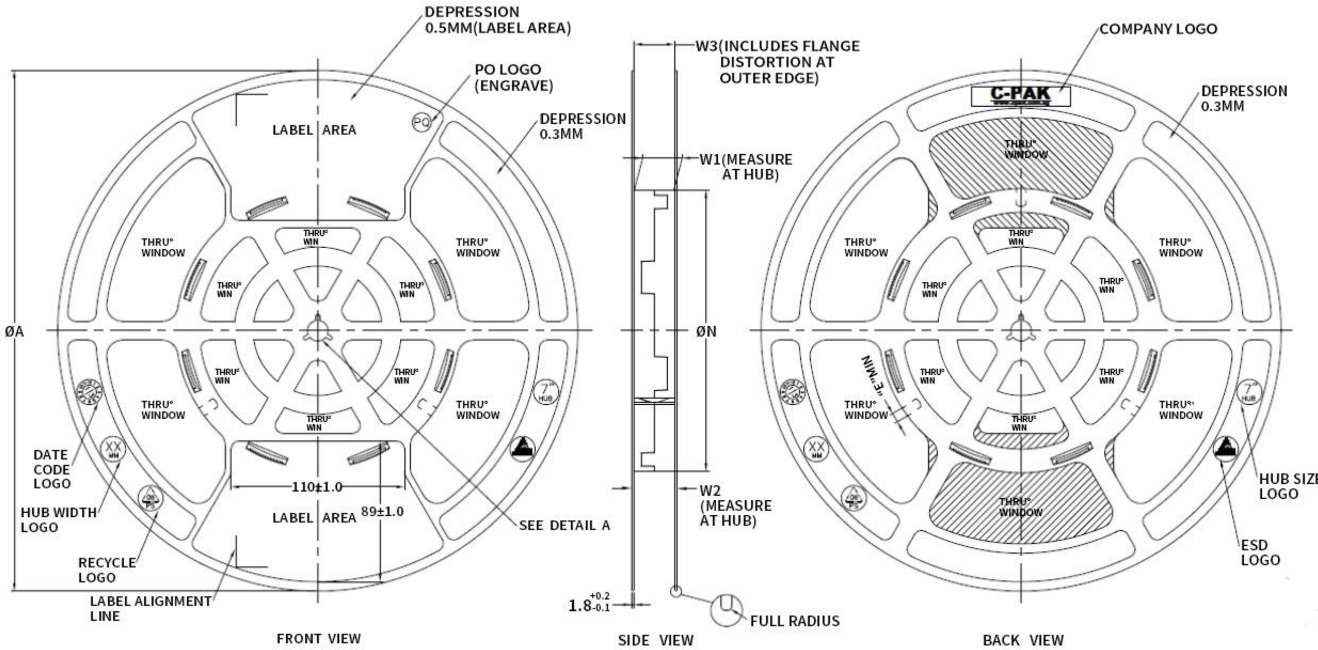
10. Order information

Part Number	Isolation Rating (kV)	Max Data Rate (Mbps)	Temperature	MSL	Package Type	Package Drawing	SPQ
NSi1050-DDBR	3	1	-40 to 125℃	3	DUB8	DUB8	800
NSi1050-DSWR	5	1	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.							

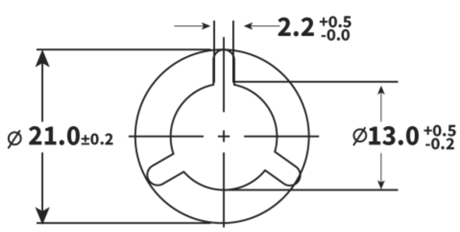
11. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSi1050	Click here	Click here	Click here	Click here

12. Tape and Reel Information



PRODUCT SPECIFICATION						
TAPE WIDTH	∅A ±2.0	∅N ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	$8.4^{+1.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT NTERFERENCE	5.5
12MM	330	178	$12.4^{+2.0}_{-0.0}$	18.4		5.5
16MM	330	178	$16.4^{+2.0}_{-0.0}$	22.4		5.5
24MM	330	178	$24.4^{+2.0}_{-0.0}$	30.4		5.5
32MM	330	178	$32.4^{+2.0}_{-0.0}$	38.4		5.5



ARBOR HOLE
DETAIL A
SCALE: 3:1

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES

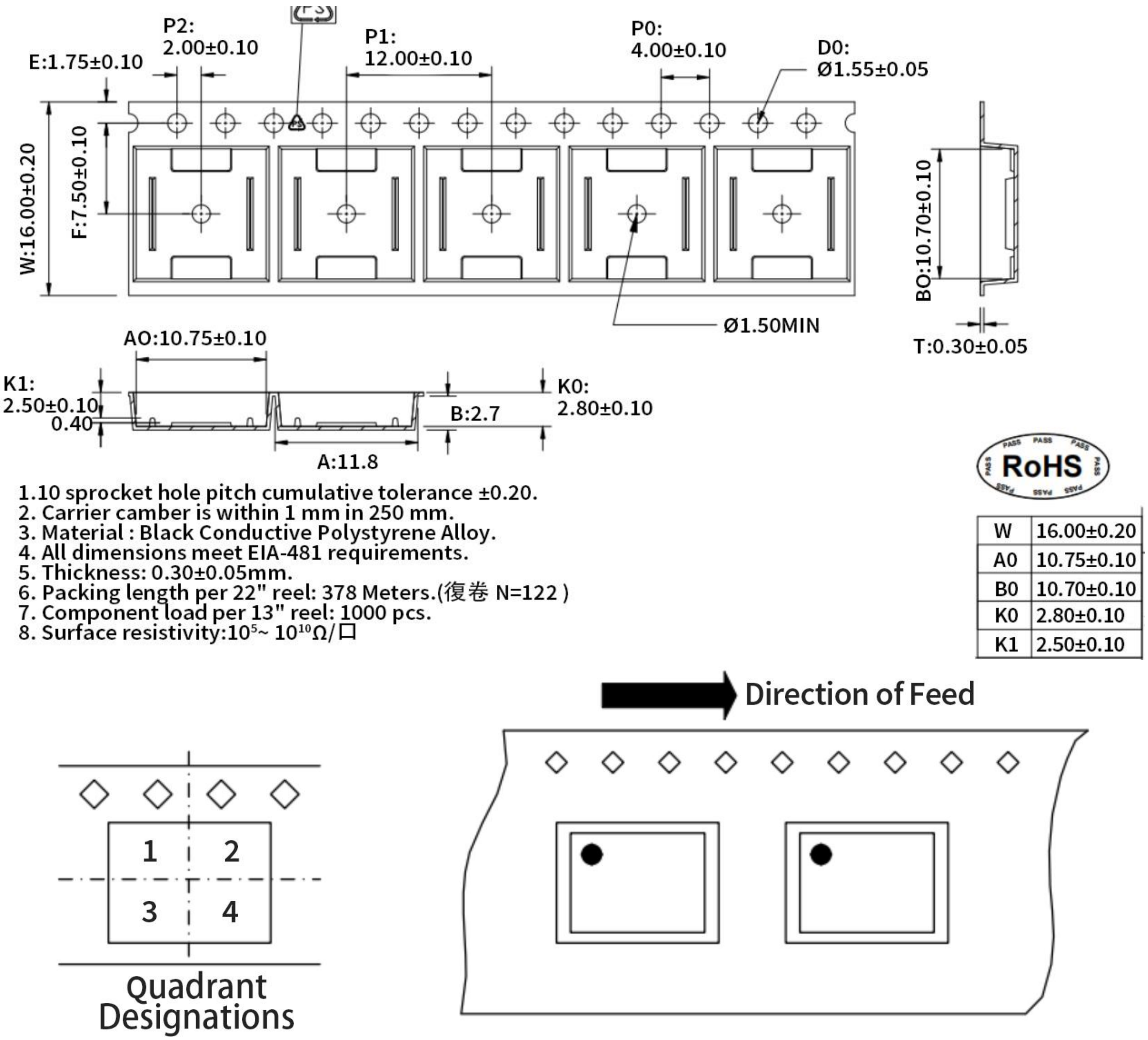
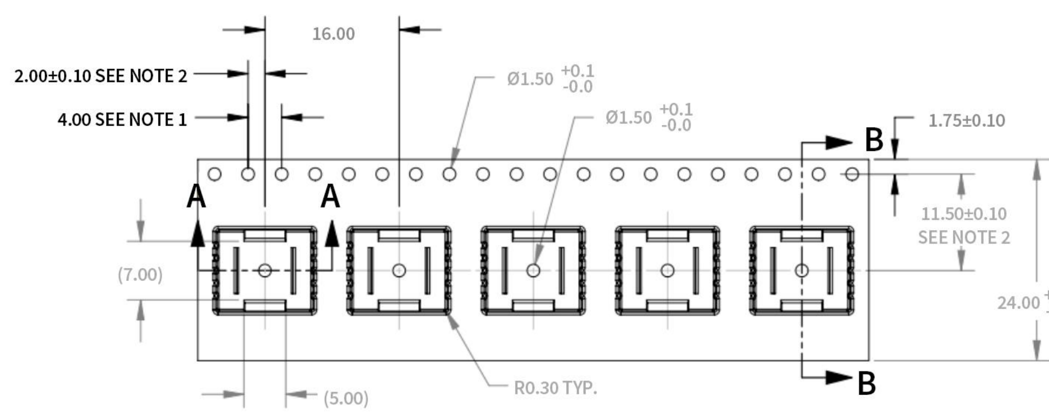
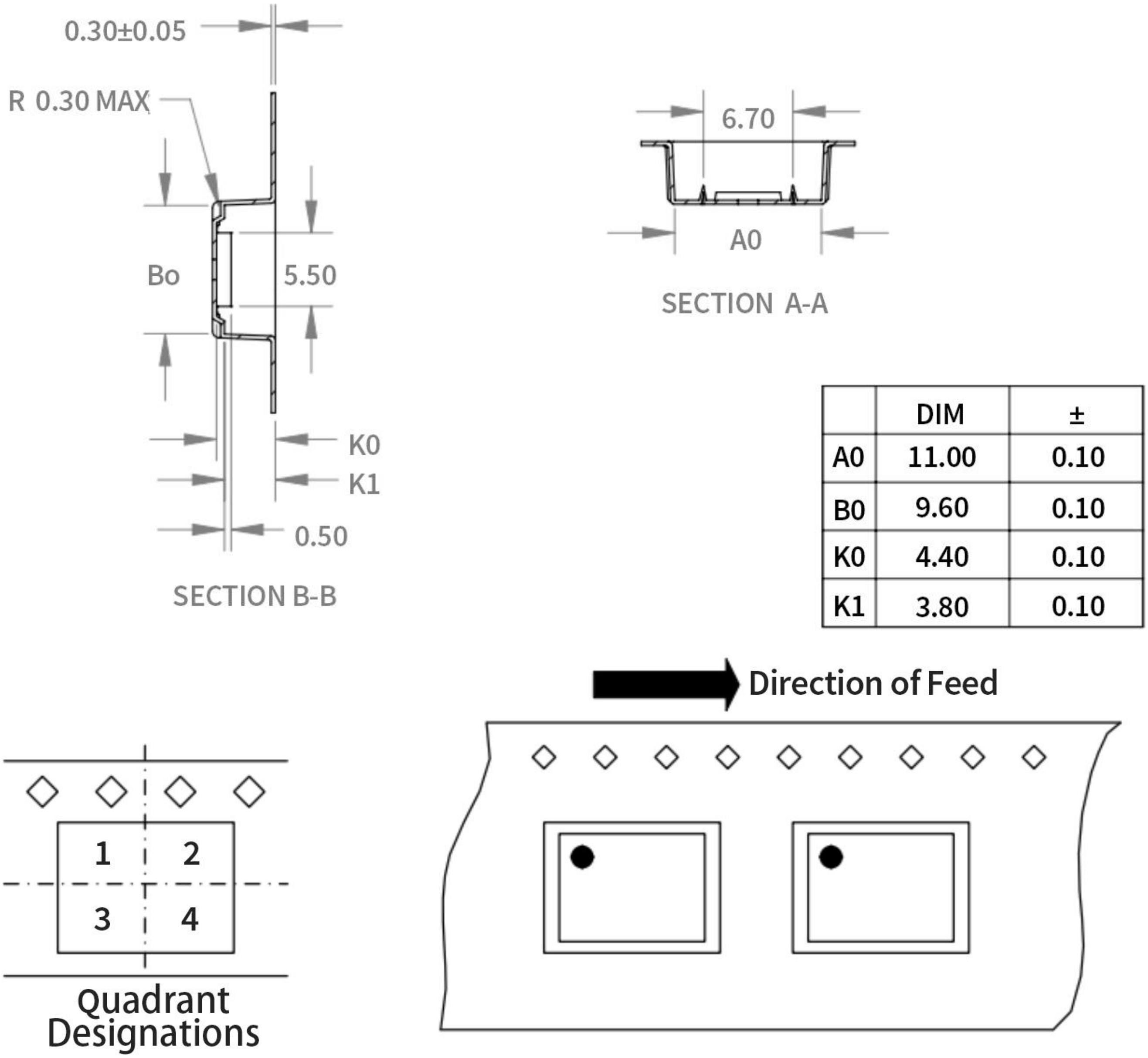


Figure 12.1 Tape and Reel Information of SOW16





	DIM	±
A0	11.00	0.10
B0	9.60	0.10
K0	4.40	0.10
K1	3.80	0.10

Figure 12.2 Tape and Reel Information of DUB8

13. Revision History

Revision	Description	Date
1.0	Initial version	2020/8/7
1.1	Changed tape and reel information	2020/12/20
1.2	Added DUB8 tape and reel information	2021/3/1
1.3	Update Regulatory information	2021/4/13
1.4	Added reel direction of feed, corrected driver and receiver delay and UL Isolation voltage	2022/6/7
1.5	Update DUB8 Package Board Layout Example	2022/8/26

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